EE221 Midterm Ex

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Welcome to the EE221 Midterm. This is a closed book examination. You may have two sheets of notes. You may also use a calculator.

Answer only 4 of the 6 problems!

Each problem is worth 25 points. Show your work; credit will be given only if the steps leading to the answer are clearly shown. You might want to indicate voltages and currents on the schematics if appropriate. Partial credit will be given for partially correct answers but only if correct intermediate steps are shown.

NOTE: Use the second approximation for all diodes!

Also assume that all clippers are stiff and clampers have a long time constant compared to the input frequency

Grading
1. 21/25
2. —
3. —
4. 5/25
5. 22/25
6. 16.5/25

Total ~~64.5~~ 65

"Of all the things that I have lost, I miss my mind the most!"

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1)

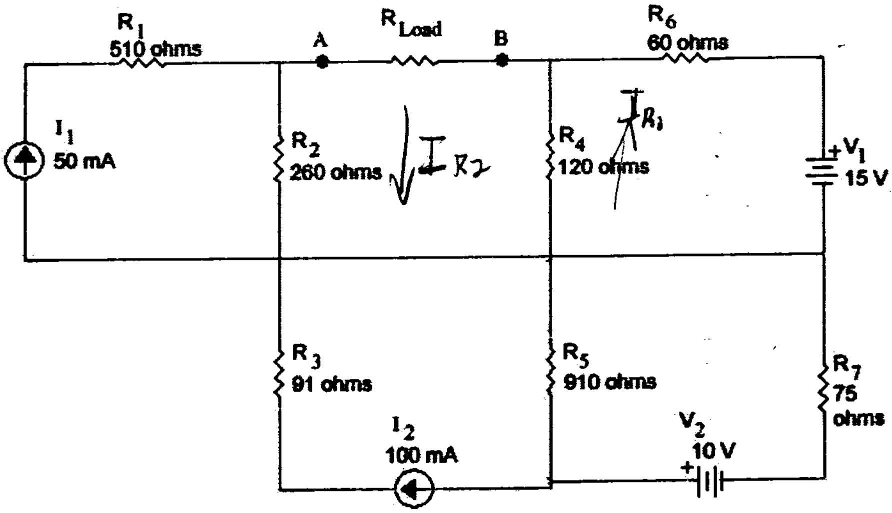
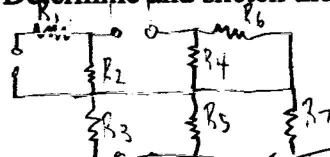


Figure 1

a) Determine and sketch the Thevenin's equivalent circuit for the output terminals A and B.

1/5

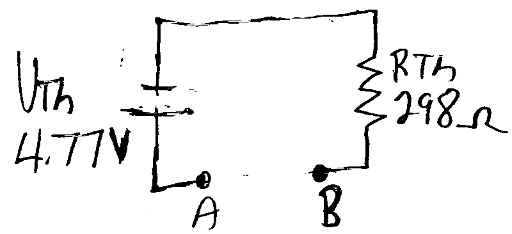


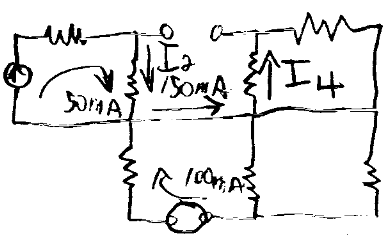
$R_{Th} = (((R_7 + R_5) // R_6) // R_4) + R_2$ ✗

$R_{Th} = (((75\Omega + 910\Omega) // 60\Omega) // 120\Omega) + 260\Omega$

$\boxed{R_{Th} = 298\ \Omega}$

The Venin Circuit

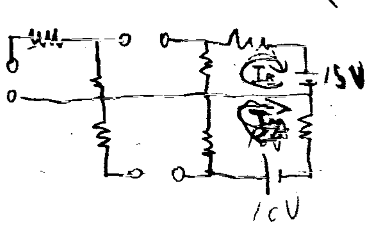




$I_{R2} = 50mA$

Using CDR

$I_{R1} = (150mA - 100mA)\left(\frac{75\Omega}{180\Omega + 75\Omega}\right) = 14.7mA$ ✗



$10V = 910\Omega I_A + 75 I_A$

$I_A = 10.15mA$

$-15V = 60\Omega I_B + 120\Omega I_B$

$I_B = 83.3mA$

$I_{R4} = 14.7mA - 83.3mA$ $= I_{R1}$

$= -68.6mA$ (opposite as shown)

$I_{R2} = 50mA$

$V_{Th} = V_{AB} = +I_{R2}(R_2) \mp I_{R1}(R_4)$

$V_{Th} = (50mA)(260\Omega) + (68.6mA)(120\Omega)$

$\boxed{V_{Th} = -4.77V}$ ← this should be pos

∴ V_B is at a lower potential ∴

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Question 1 Continued

b) At what value of load resistance will 600 μA flow through the load?

R_{Load} = 7K652 Ω

5

$V = IR$

$I = \frac{V}{R} = \frac{V_{Th}}{R_{Th} + R_L} =$

$R_L = \frac{V_{Th}}{I} - R_{Th} = \frac{4.77V}{600\mu A} - 298\Omega$

$R_L = 7652\Omega = 7K652\Omega$

c) At what value of load resistance is maximum power transferred?

R_{Load} = 298 Ω

5

$R_{Load} = R_{Th}$ at max power

d) What would be the minimum load resistance if this Thevenin's equivalent circuit was to be a stiff voltage supply?

$R_{Load(min)}$ = 29K8 Ω

5

Stiff voltage supply $R_S < 0.01 R_L$

$R_L > 100 R_S$

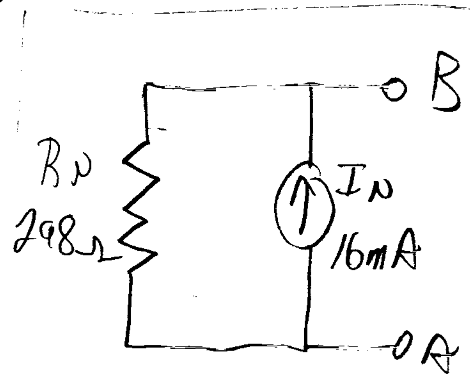
$R_L > 100(298\Omega)$ → $R_L > 29K8\Omega$

e) What is the Norton's equivalent circuit?
(Provide a circuit sketch as well)

5

$R_N = R_{Th} = \boxed{298\Omega}$

$I_N = \frac{V_{Th}}{R_{Th}} = \frac{4.77V}{298\Omega} = \boxed{16mA}$



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2) **(Use the second approximation of the diode!)**

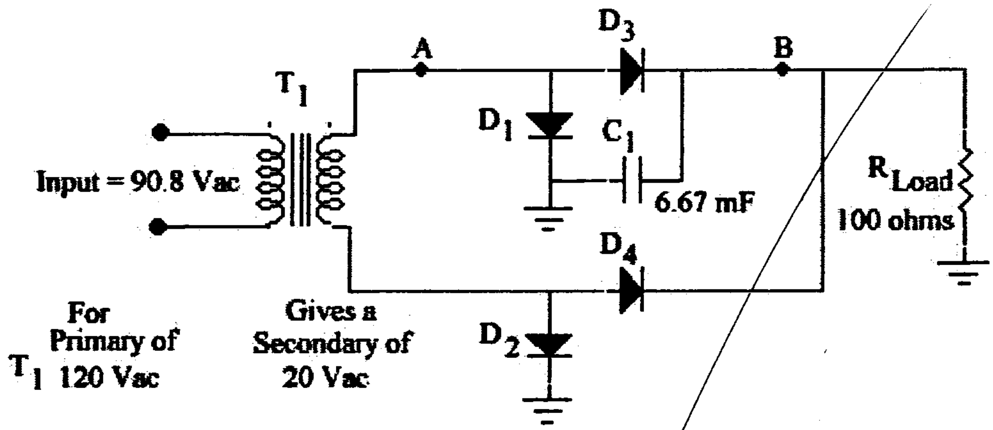

Figure 2

a) What is the peak or maximum voltage across the load?

V_{Load} = ____________

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Question 2 Continued

b) What is the peak to peak ripple voltage at the load?

V_{ripple} = ____________

c) What rectifier configuration is this supply?

d) Using the graph on the next page, sketch the waveform at point 'A'. Also on the same graph sketch the resulting waveform at point 'B' both with and without the capacitor in circuit.
(You must indicate which waveform is which along with voltage levels.)

Please try to be neat! A sloppy diagram may lead to a misinterpretation and lost marks.

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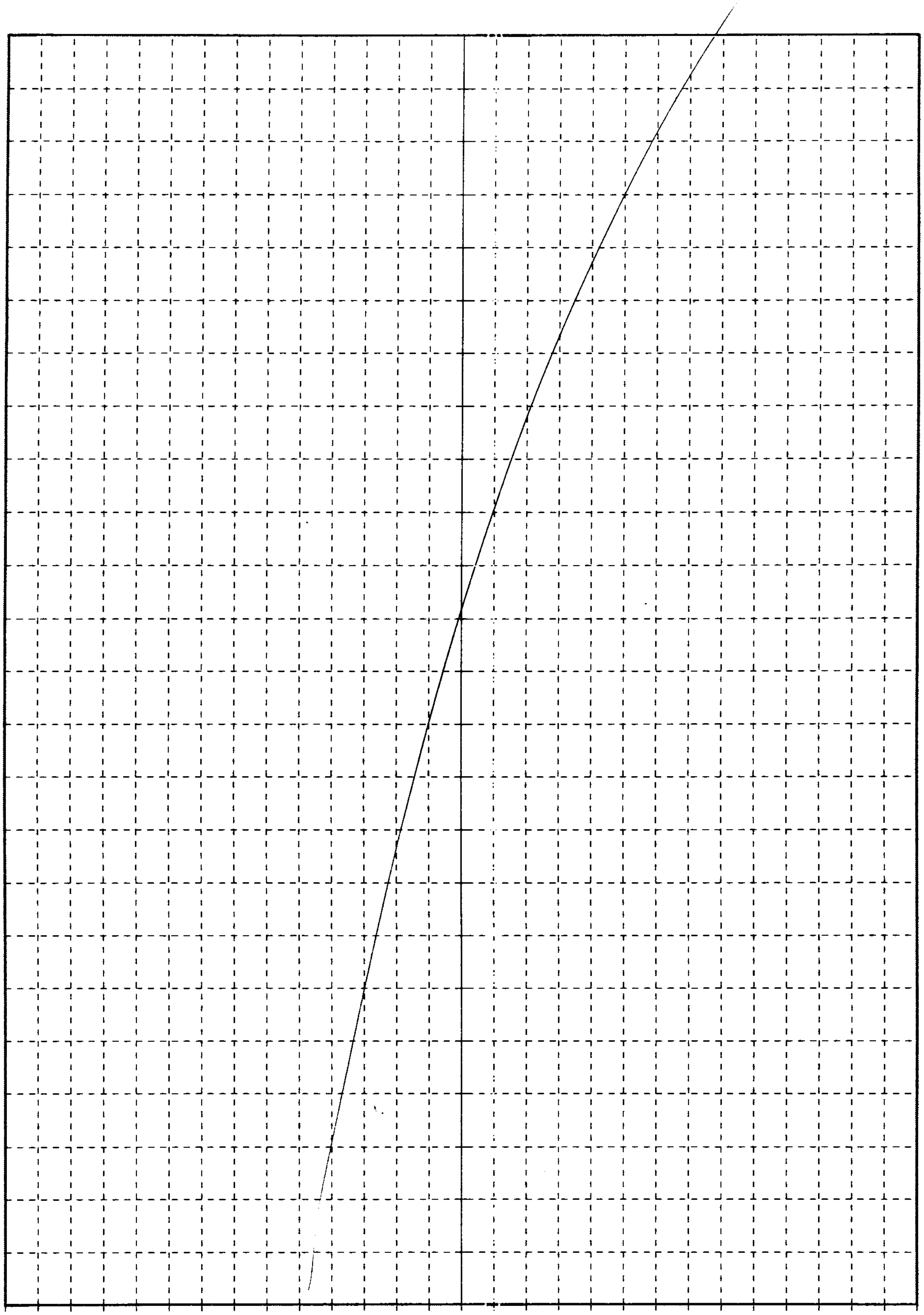

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3) **(Use the second approximation of the diode!)**
Sketch the waveform at each terminal, A, B, C, and D on the supplied graphs.

Please try to be neat! A sloppy diagram may lead to a misinterpretation and lost marks.

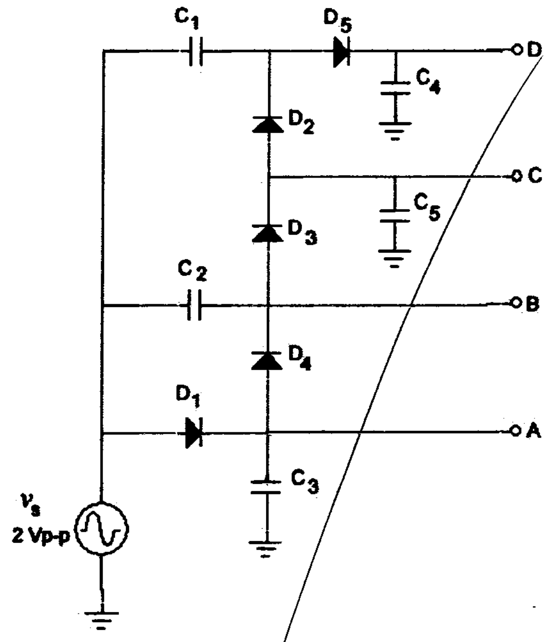

Figure 3

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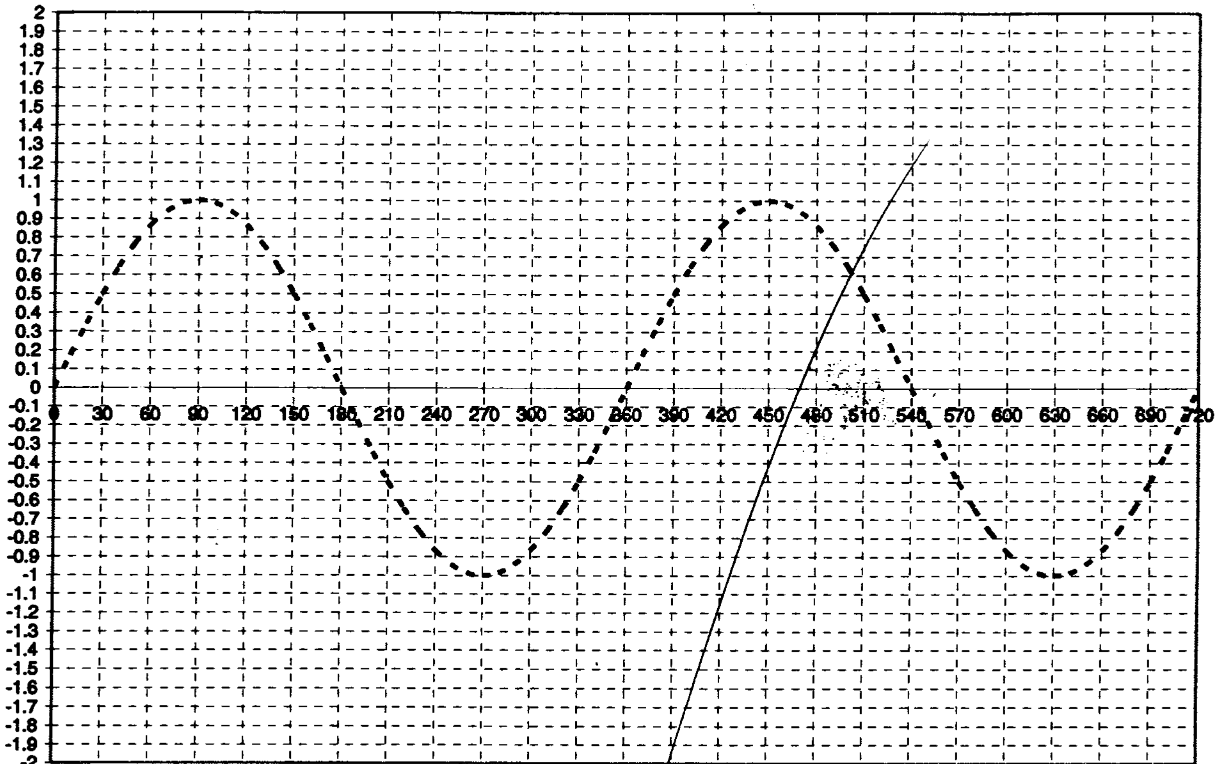
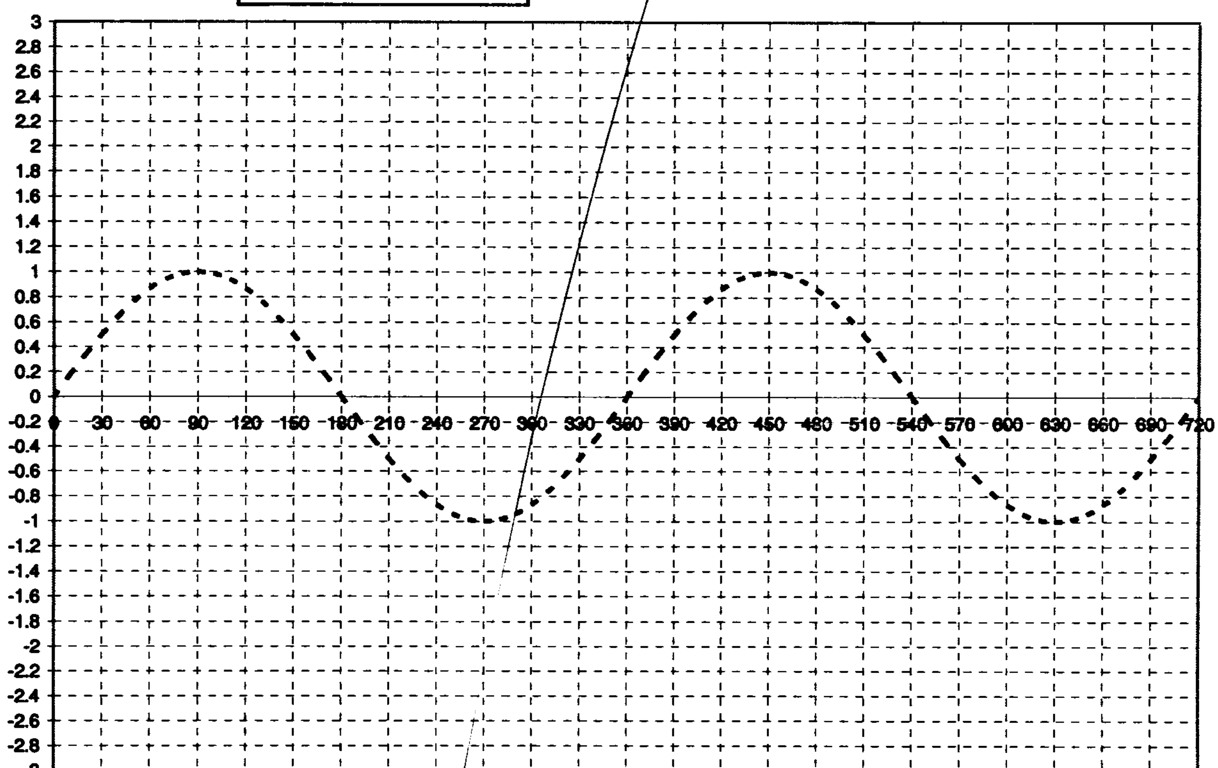
Question 3 Continued



Graph 1 for V_A

Vs



Graph 2 for V_B

Vs

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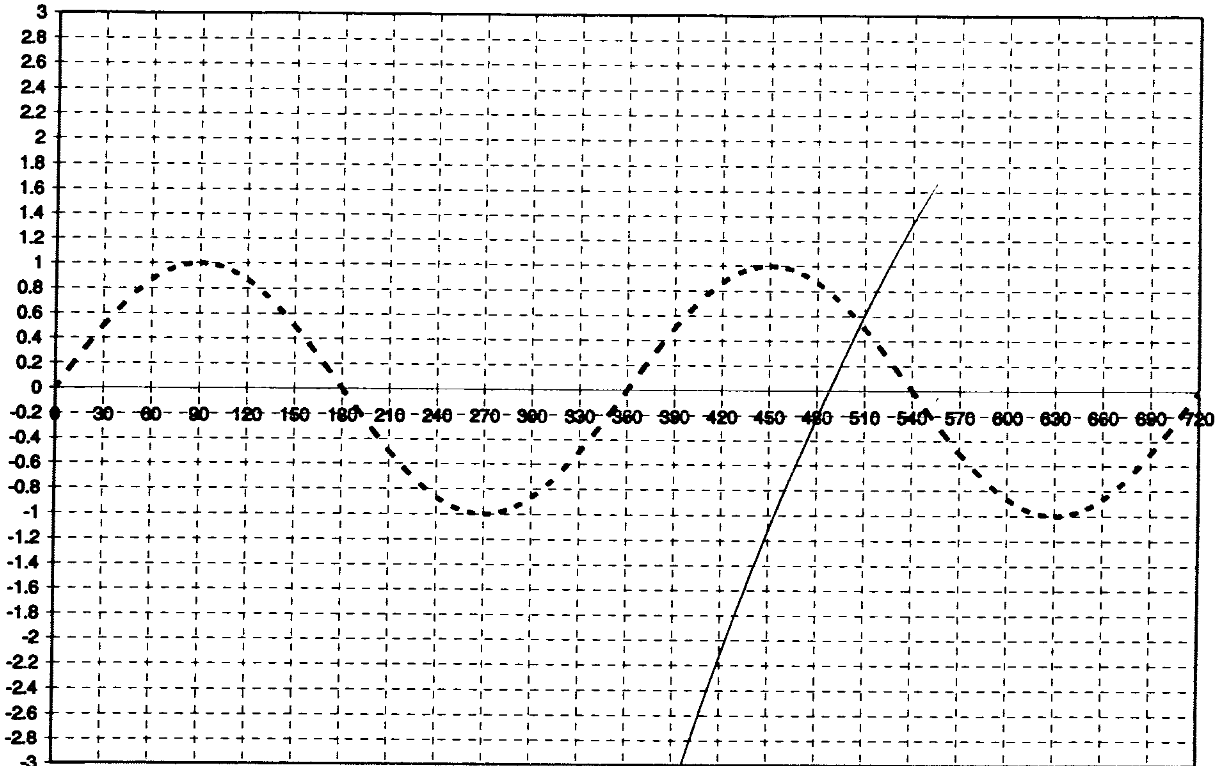
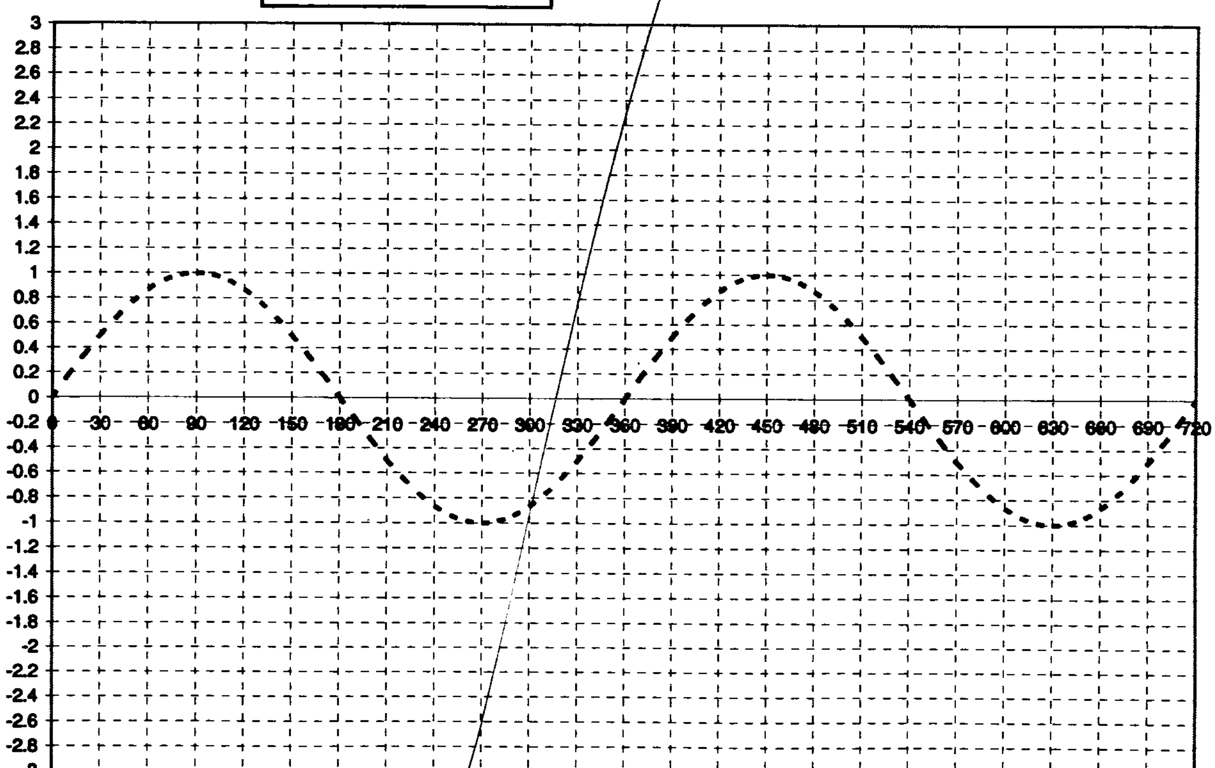
Question 3 Continued



Graph 3 for V_C



Graph 4 for V_D

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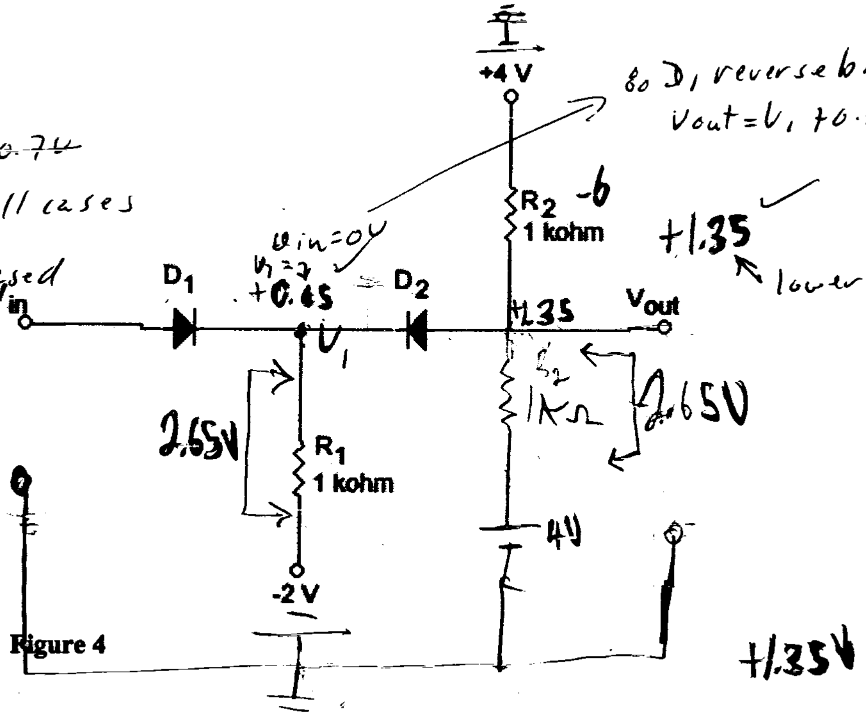
4) **(Use the second approximation of the diode!)**
With the given V_{in} sketch V_{out} on the same graph.

Please try to be neat! A sloppy diagram may lead to a misinterpretation and lost marks.

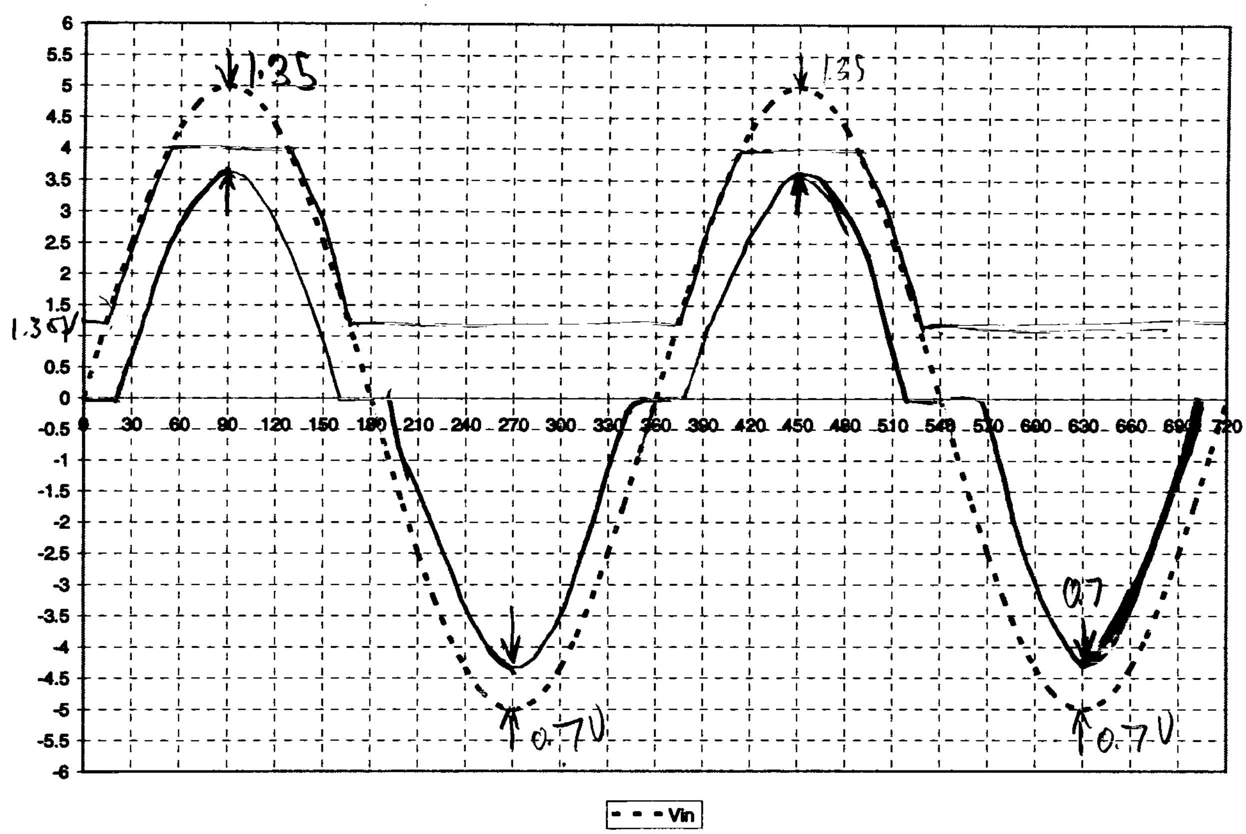
$V_{out} = V_1 + 0.7V$
$V_1 = V_{in} - 0.7V$
$V_{out} = V_{in}$ ~~$-0.7V + 0.7V$~~
but not for all cases

$V_1 > 3.3V$ D_2 reverse biased
$\therefore V_{out} = 4V$
upper limit

so D_1 reverse biased
$V_{out} = V_1 + 0.7V = 1.35V$
+1.35
lower limit.



5/25



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5) **(Assume $\beta = 100$, $V_{BE} = 0.7$ V and $V_{CE(sat)} = 0.3$ V)**

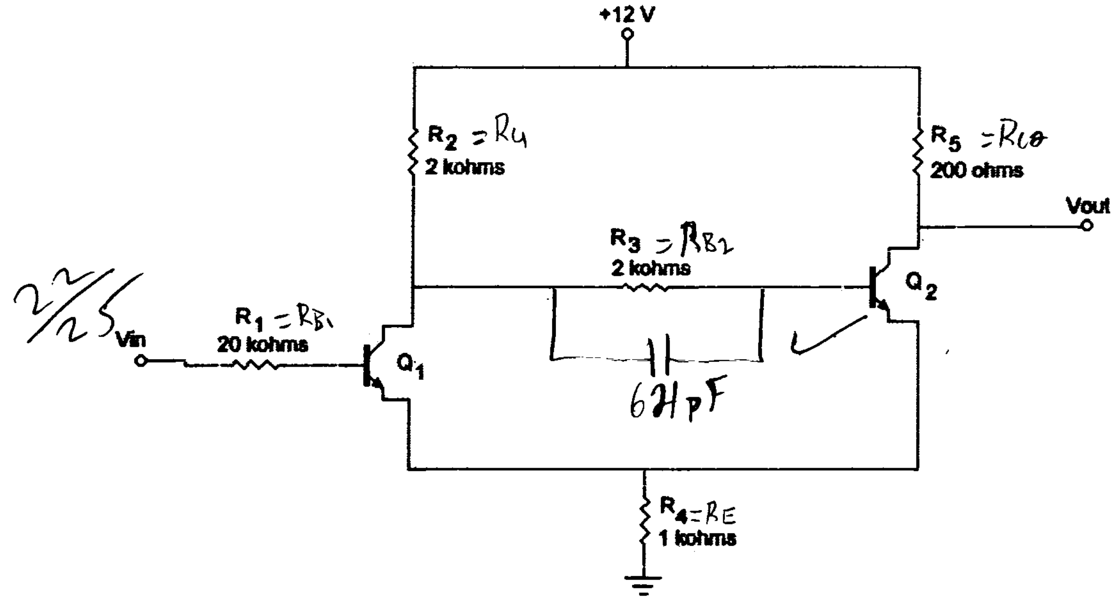

Figure 5

$pF = 1\times10^{-12}$

Find the following for the above transistor Schmitt trigger.

a) Determine the:

- Upper Trip Point? UTP = 8V ✗
- Lower Trip Point? LTP = 4V ✓
- Hysteresis Voltage? V_H = 4V ✗✓

4.25 / 6.25

UTP

$$V_{RE} = \frac{R_E}{R_E + R_{C2}}(V_{cc}) = 12\,V\left[\frac{(1k\Omega)}{(1k\Omega + 500\Omega)}\right] = \boxed{8\,V}$$ ✗

?

LTP

$$V_{RE} = \left(\frac{R_E}{R_E + R_{C1}}\right) V_{cc} = 12\,V\left[\frac{1k\Omega}{1k\Omega + 2k\Omega}\right] = \boxed{4\,V}$$

V_H

$$V_H = U_{TP} - L_{TP} = 8V - 4V = \boxed{4V}$$ ✗✓

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Question 5 Continued

b) It is determined that a capacitor can be used in order to increase the switching time.

6.25 On the circuit diagram sketch where this capacitor is to be connected.

c) If this was a 621 pF capacitor, what would the maximum switching frequency be?

F_{max} = 700 KHz

6.25

$$C_{max} = \frac{t_{re}}{2.3R}$$

Since $t_{re} = \frac{1}{f_{max}}$ & $R = R_{B2} // R_{C1}$

we get

$$f_{max} = \frac{1}{(C_{max})2.3R} = \frac{1}{(621 \times 10^{-12} F)(2.3)(2k\Omega // 2k\Omega)}$$

$$\boxed{f_{max} = 700 \text{ KHz}}$$

d) List two advantages the transistor Schmitt Trigger has over a Basic Transistor Switch.

1) With a schmitt Trigger the circuit will stay on until it drops below LTP and won't turn on until it rises above UTP.

3.25/6.25

X 2) This keeps the input the same as the output, with a normal trigger the output would be inverted.

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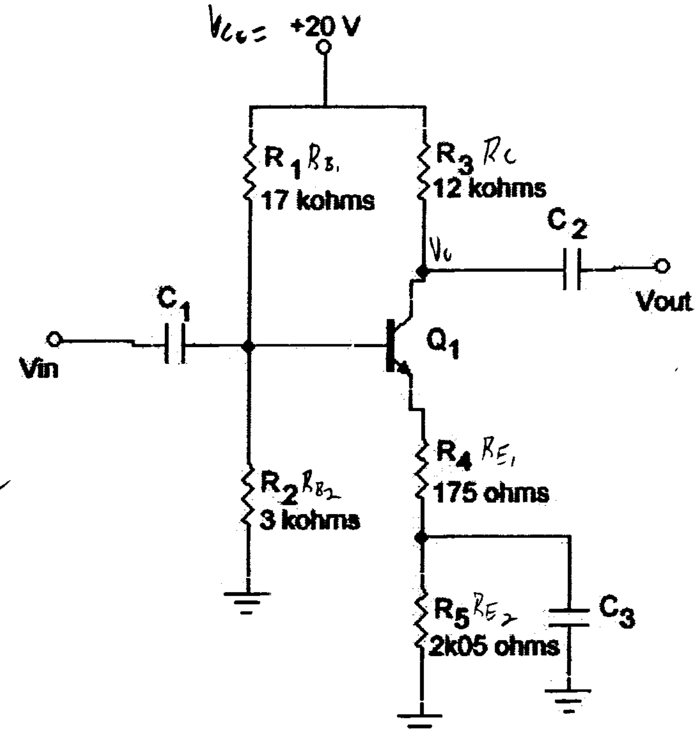
6) **(Assume $\beta = 100$, $V_{BE} = 0.7$ V, $V_{CE(sat)} = 0.3$ V, and at room temperature (300 °K))**



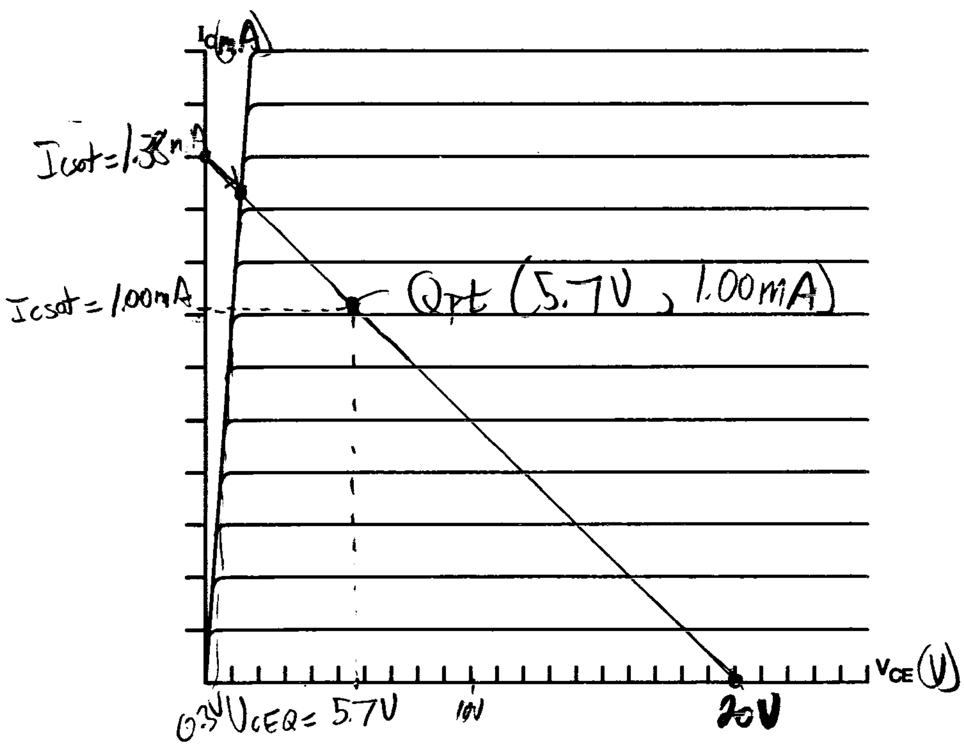
16.5 / 25

Figure 6

a) Draw the DC load line and determine the Q point.
(Use the supplied transistor curve and label the X and Y axis' values)

I_{CQ} = 1.00mA ✗ V_{CEQ} = 5.7V ✓

3/5



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Question 6 Continued
Page for Q point calculations

$$V_B = V_{cc}\left(\frac{R_2}{(R_1+R_2)}\right) = 20V\left(\frac{3k\Omega}{7k\Omega+3k\Omega}\right) = \underline{3V}$$

$$V_E = 3V - 0.7V = \underline{2.3V}$$

$$I_E = \frac{V_E}{R_{E1}+R_{E2}} = \frac{2.3V}{175\Omega+2k05\Omega} = \underline{1.03mA}$$

$$I_{CQ} = \frac{\beta}{(\beta+1)} I_E = \frac{100}{101}(1.03mA) = \boxed{1.02mA}$$

$$V_C = V_{cc} - I_C R_C = 20V - (1.00mA)(12k\Omega) = 8V$$

$$V_{CEQ} = V_C - V_E = 8V - 2.3V = \boxed{5.7V}$$ with your I_C

$$I_{Csat} = \frac{V_{cc} - \overset{0V}{0.3V}}{R_3+R_4+R_5} = \frac{20V - 0.3V}{12k\Omega+175\Omega+2k05\Omega} = 1.38mA$$

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Question 6 Continued

b) Determine the input impedance (Zin), output impedance (Zout) and voltage gain (Av).

Zin = 2K26Ω Zout = 12KΩ Av = -60

4.5/5

$Z_{OUT} = R_C = 12K\Omega$

$r'_e = \frac{0.02585V}{I_E} = \frac{0.02585V}{1.03mA} = 25.1\Omega$

$Z_{in} = R_1 // R_2 // \beta(r'_e + R_{E1}) = 17K\Omega // 3K\Omega // 100(25.1\Omega + 175\Omega) = 2K26\Omega$

$A_V = -\frac{R_C}{r'_e + R_{E1}} = -\frac{12K\Omega}{(25.1\Omega + 175\Omega)} = -60$

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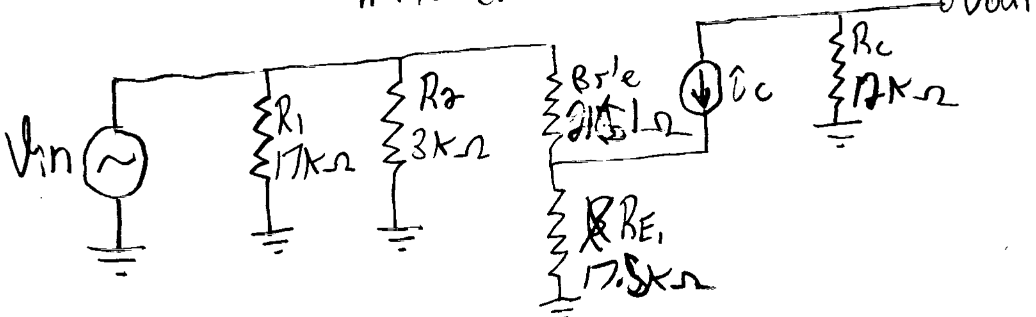
Question 6 Continued

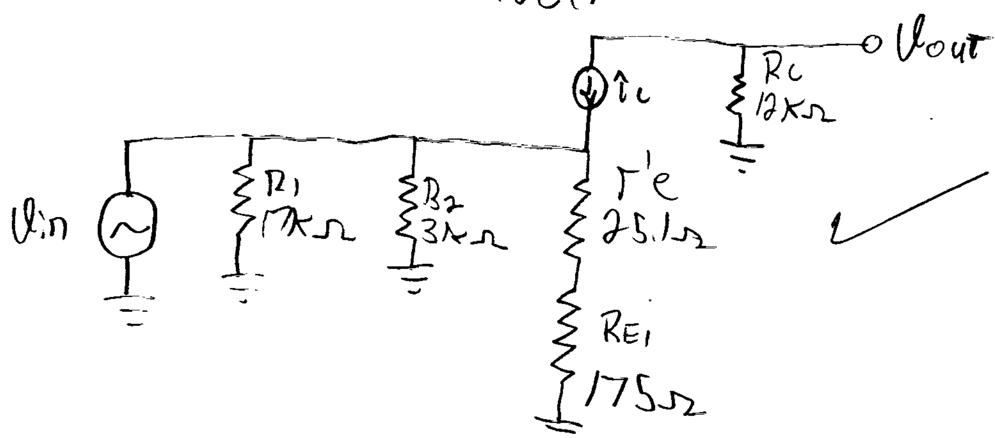
c) Sketch the T and π transistor ac models for this circuit.
(Remember to label all components)

'π model'



4/5

'T model'



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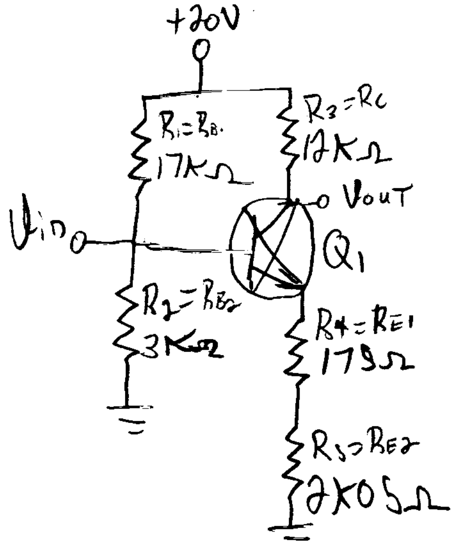
Question 6 Continued

d) Sketch the DC transistor model for this circuit.
(Remember to label all components)



DC model not circuit.

0/5

e) Is this a stiff voltage divider bias?
(You must show proof to support your answer)

For Stiff VDB we need to satisfy $R_1 // R_2 < 0.01 \beta R_E$

$R_1 // R_2 = 17k\Omega // 3k\Omega = 2K55\Omega$

$(0.01)(100) R_E = 1(R_{E1} + R_{E2}) = 1(175\Omega + 2k05\Omega) = 2k25\Omega$

$\therefore$ Since $R_1 // R_2 \nless R_E$

$2550\Omega \nless 2250\Omega$

5

The voltage Divider is not stiff